1. (Currently Amended) A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region; and

source and drain regions laterally adjacent said channel region,

wherein said channel region includes an extension into said source and drain regions.

[an isolation layer below said second gate,]

[wherein said first gate and said second gate are self-aligned and electrically separated from each other,]

[wherein a material composition of said second gate is independent of a material composition of said isolation layer.]

2. (Original) The transistor of claim 1, wherein said first gate comprises a different doping concentration that said second gate.

3. (Original) The transistor of claim 1, wherein said first gate comprises a different doping species than said second gate.

4. (Original) The transistor of claim 1, further comprising a first gate dielectric below said first gate and a second gate dielectric above said second gate.

5. (Original) The transistor of claim 1, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

6. (Original) The transistor of claim 1, wherein said first gate comprises a different material than said second gate.

7. (Original) The transistor of claim 1, wherein said first gate comprises a different thickness than said second gate.

8. (Original) The transistor of claim 1, wherein said first gate, said second gate and said channel region form a planarized structure.

9. (Original) The transistor of claim 4, wherein said first gate dielectric comprises a different material than said second gate dielectric.

10. (Original) The transistor of claim 4, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

11. (Currently Amended) A semiconductor chip having at least one transistor, said transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region; [and]

a first gate dielectric below said first gate;

a second gate dielectric above said second gate;

source and drain regions laterally adjacent said channel region; and

source and drain dielectrics between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

[an isolation layer below said second gate,]

[wherein said first gate is self-aligned with and comprises a different material than said second gate].

12. (Original) The semiconductor chip of claim 11, wherein said first gate and said second gate have different dopant concentrations.

13. (Original) The semiconductor chip of claim 11, wherein said first gate and said second gate have different dopant species.

14. (Cancelled).

15. (Currently Amended) The semiconductor chip of claim [14] 11, wherein said first gate dielectric comprises a different material than said second gate dielectric.

16. (Currently Amended) The semiconductor chip of claim [14] 11, wherein said first gate dielectric comprises a different thickness than said second gate dielectric.

17. (Original) The semiconductor chip of claim 11, wherein said first gate has a first conductive contact and said second gate has a second conductive contact and said first conductive contact and said second conductive contact are coplanar.

18. (Original) The semiconductor chip of claim 11, wherein said first gate and said second gate are electrically separated.

19. (Original) The semiconductor chip of claim 11, wherein said first gate and said second gate have different thicknesses.

20. (Original) The semiconductor chip of claim 11, wherein said first gate, said second gate and said channel region form a planarized structure.

21-43. (Cancelled).

44. (Previously Presented) A transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region;
an isolation layer below said second gate; and

source and drain regions laterally adjacent said channel region,

wherein said source and drain regions are self-aligned with said first gate and said second gate, such that said source and drain regions do not horizontally overlap said first gate or said second gate, and

wherein said first gate and said second gate are electrically separated from each other, and

wherein said channel region includes an extension into said source and drain regions.

45-54. (Cancelled).

Please add the following claim:

55. (New) A transistor comprising:

a substrate having a crystal orientation;

a single crystal channel above said substrate, wherein the crystal orientation of said single crystal channel is independent of said crystal orientation of said substrate;

a first gate above said single crystal channel; and

a second gate below said single crystal channel.